REMARKS

Favorable reconsideration of this application in view of the foregoing amendments and remarks to follow and allowance of the claims of the present application are respectfully requested.

Applicants have amended Claim 1 to include language that wherein said first layer of metal and said second layer of metal are not interconnected by a via. Support for this amendment to Claim 1 can be found at paragraphs [0018] and [0019] of the present application.

Applicants have also amended Claim 2 to include language that wherein said second layer of metal and said third layer of metal are not interconnected by a via. Support for this amendment to Claim 2 can be found at paragraphs [0018] and [0019] of the present application.

To be consistent with the newly amended Claims 1 and 2, applicants have further amended Claims 19 and 20, which are directed to a method of forming a semiconductor structure. Support for the amendments to Claims 19 and 20 can be found at paragraphs [0018] and [0019] of the present application.

In addition, applicants observe that Claim 7 was also amended to delete the word "said".

Since the above amendments to the claims do not introduce new matter into the application, entry thereof is respectfully requested.

Claim 7 stands rejected under 35 U.S.C. §1 12, first paragraph, as allegedly failing to comply with the written description requirement. Specifically, the Examiner alleges that there is inadequate description in the disclosure for at least one wiring region that lies to the periphery of the metal stacked inductor.

Concerning the written description requirement, a description as filed is presumed to be adequate, unless or until sufficient evidence or reasoning to the contrary has been presented by the examiner to rebut the presumption. *In re Marzocchi*, 439 F.2d 220, 224, 169 USPQ 367, 370 (CCPA 1971). Applicants respectfully submit that the Examiner fails to establish a *prima facie* case of lack of written description for the following reasons. In the present application, paragraph 31 discloses that "other areas, such as wiring areas can lay to the periphery of the inductor areas shown." Further, paragraph 60 of the specification states that "it should be noted that in other areas of the interconnect structure such as, for example, in the wiring areas, the second layer of metal 54 serves as a via interconnecting two metal wires; the two metal wires are composed of the first layer of metal 52 and the third layer of metal 56." In view of the above, one ordinarily skilled in the art would readily ascertain that the applicants were in possession of the invention of Claim 7, i.e., at least one wiring region that lies to the periphery of the metal stacked inductor, wherein in the at least one wiring region the second layer of metal serves as a via interconnecting two metal wires, as of the filing date of the application.

Applicants therefore submit that Claim 7 is adequately supported by the specification. Hence, reconsideration and withdrawal of the rejection under the §112, first paragraph, is respectfully requested.

Claims 1-6, 19 and 20 stand rejected under 35 U.S.C. §102(b), as allegedly anticipated by U.S. Patent No. 6,395,637 to Park, et al. (hereinafter "Park"). Specifically, the Examiner alleges that Fig. 4E of Park teaches a metal stacked inductor comprising at least one first layer of metal (12) and a second layer of metal (15) located directly on top of the first layer of metal.

It is axiomatic that anticipation under §102 requires that the prior art reference discloses each and every element of the claim to which it is applied. *In re King*, 801 F.2d, 1324, 1326, 231 USPQ 136, 138 (Fed. Cir. 1996). Thus, there must be no differences between the subject matter of the claim and the disclosure of the prior art reference. Applicants respectfully submit that Park does not anticipate Claims 1-6, 19 and 20 of the present application since Park does not teach the claimed semiconductor structure recited in Claim 1 or the method recited in Claim 19. Specifically, the applied reference dose not disclose a metal stacked inductor comprising at least one first layer of metal which serves as an upper metal wire in the semiconductor structure and a second layer of metal located directly on top of the first layer of metal, wherein said first layer of metal and said second layer of metal are not interconnected by a via.

Park (Fig. 4E) discloses a metal stacked inductor comprising three layers of metal, i.e., the first layer of metal (12), the second layer of metal (15) and the third layer of metal (21). According to Fig. 4E and additional description in the specification (lines 47-51, lines 59-61, column 5; and lines 9-11, column 6), there are a dielectric layer (13) and a via hole (14) between the first layer of metal (12) and the second layer of metal (15). In other words, the second layer of metal (15) is not located directly on top of the first layer of metal (12), instead, the second layer of metal (15) interconnects the first layer of metal (12) by a via. Further, there are a dielectric layer (17) and a via hole (18) filled with Al between the second layer of metal (15) and the third layer of metal (21) (Fig. 4E; lines 56-61, column 5; and lines 9-11, column 6). In other words, the third layer of metal (21) is not located directly on top of the second layer of metal (17). Instead, the third layer of metal (21) interconnects the second layer of metal (17) by a via. To the contrary, the presently amended Claim 1 specifies that the second layer of metal is located

directly on top of the first layer of the metal, and the first layer of metal and the second layer of metal are not interconnected by a via. The presently amended Claim 2 also specifies that the third layer of metal is located directly on top of the second layer of the metal, and the second layer of metal and the third layer of metal are not interconnected by a via. Further, the present specification states that the substantially low sheet resistance of the dual and tri-metal inductors of the present invention is achieved because no via is used interconnecting the multiple layers of metal. See paragraphs [0018] and [0019]. Since Park fails to teach one essential limitation of the present invention, namely no via between the layers of metal, Park does not anticipate Claims 1-2. Along the same line of argument, Park does not anticipate Claims 3-6, which depend from Claims 1 and include every limitation of Claim 1. Claims 19 and 20 are directed to the methods of forming the claimed semiconductor structure. Inasmuch as the claimed semiconductor structure is novel over Park, the methods of forming the inventive structure are novel as well.

The rejection under 35 U.S.C. §102(b) has been obviated; therefore reconsideration and withdrawal thereof is respectfully requested.

Claims 8-18 stand rejected under 35 U.S.C. §103(a), as allegedly unpatentable over Park in view of U.S. Patent No. 6,639,298 to Chaudhry, et al. (hereinafter "Chaudhry"). Particularly, the Examiner alleges that Park teaches substantially the entire claimed structure of Claim 1 except explicit stating that the first layer of metal is comprised of a low resistivity conductive material having a resistivity of about 3.0 micro-ohm*cm or less, and Chaudhry teaches using copper in the process of forming a multi-layer inductor structure. The Examiner therefore concludes that it would have been obvious to one of ordinary skill in the art at the time the invention was made to use copper in the structure of Park as taught by Chaudhry in order to form a high Q inductor.

Applicants respectfully submit that Claims 8-18 of the present application are not rendered obvious by Park in view of Chaudhry since the applied references do not teach or remotely suggest applicants' claimed semiconductor structure. Specifically, the applied references, solely or in combination, do teach or suggest the claimed metal stacked inductor comprising at least one first layer of metal which serves as an upper metal wire in the semiconductor structure and a second layer of metal located directly on top of the first layer of metal, wherein said first layer of metal and said second layer of metal are not interconnected by a via.

As discussed above, the principle reference, Park, discloses a metal stacked inductor comprising three layers of metal. However, there are a dielectric layer and a via hole between the metal layers. In other words, the second layer of metal connects to the first layer of metal by a via, and the third layer of metal connects to the second layer of metal by a via. In contrast, Claim 1 of the present invention specifies that the second layer of metal and the first layer of the metal are not interconnected by a via, and Claim 2 of the present invention specifies that the third layer of metal and the second layer of the metal are not interconnected by a via. The other reference, Chaudhry, discloses an integrated circuit inductor having a plurality of insulating layers and a plurality of metallization layers, which differs considerably from the present inventive metal stacked inductor.

Furthermore, neither Park nor Chaudhry remotely suggests the present semiconductor structure. Park emphasizes that the high performance of the inductor is achieved by fully filling the via hole and the via recesses with the Al layer to increase the actual thickness of the inductor coil (lines 9-21, column 6), and Chaudhry specifically teaches that the desirable low-resistance (and thus high Q) of the inductors is achieved by using a dual damascene process

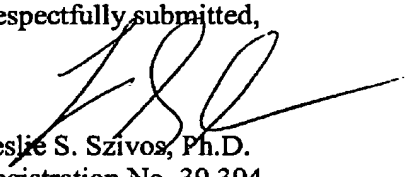
to form such an inductor (lines 56-67, Column 2). Notably, the present specification states that the high performance of the claimed inventive inductor having substantially low sheet resistance is achieved because no via is used interconnecting the multiple layers of metal. See paragraphs [0018] and [0019].

The §103(a) rejection also fails because one ordinarily skilled in the art, in view of Park and Chaudhry, would not be motivated to modify the disclosed semiconductor structure to include applicants' claimed metal stacked inductor comprising at least one first layer of metal which serves as an upper metal wire in the semiconductor structure and a second layer of metal located directly on top of the first layer of metal, wherein said first layer of metal and said second layer of metal are not interconnected by a via. Thus, there is no motivation provided in the applied references, or otherwise of record, to make the modification mentioned above. "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." In re Vaeck, 947 F.2d, 488, 493, 20 USPQ 2d. 1438, 1442 (Fed.Cir. 1991).

The rejection under 35 U.S.C. §103 has been obviated; therefore reconsideration and withdrawal thereof is respectfully requested.

Thus, in view of the foregoing remarks, it is firmly believed that the present case is in condition for allowance, which action is earnestly solicited.

Respectfully submitted,



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